REMARKS

Applicant appreciates the Examiner's thorough examination of the subject application and requests reconsideration of the subject application based on the foregoing amendments and the following remarks.

Claims 1-13 are pending in the subject application and all of these claims stand rejected under 35 U.S.C. §103.

Claims 14-19 were added to claim more distinctly embodiments of Applicant's invention. Claims 20 and 21 were added to more distinctly claim aspects/ embodiments of Applicant's invention. The amendments to the claims are supported by the originally filed disclosure.

35 U.S.C. §103 REJECTIONS

Claims 1-13 stand rejected under 35 U.S.C. §103 as being unpatentable over Suzuki et al. [USP 6,445,367; "Suzuki"] in view of Yamaguchi et al. [USP 6,184,851; "Yamaguchi"].

As grounds for the rejection the above-referenced Office Action asserts that Suzuki teaches a control circuit (103) through which an image signal enters from the outside and which generates control signals, Tscan and Tmry, that are applied to a latch circuit (105). It is further asserted that the latch circuit (105) is used as a memory circuit for storing one line of the image data for a certain period of time only. It also is asserted that Suzuki teaches a shift register that is used for converting the image data, which enters serially in a time series to parallel signals every line of the image. It also is acknowledged that Suzuki does not teach serial to parallel converting means for reading a

signal of serial data from storage means and producing as parallel data such that data from the storage means includes digital data including all pulses representative of all rise and fall timings.

It is additionally asserted in the Office Action that Yamaguchi teaches an electron-emitting device with a memory incorporating waveform characteristics, which includes the rise time Tr and the fall time Tf. It also is asserted that Yamaguchi also teaches serial to parallel conversion of data corresponding to electron emitting device where the output from the shift register is shown as N parallel signals.

It is thus concluded in the Office Action that it would have been obvious to one skilled in the art to modify the image forming apparatus disclosed in Suzuki to include Yamaguchi's shift register. The suggested motivation being that the shift register taught in Yamaguchi equivalently performs the desired serial to parallel conversion of the data. Applicant respectfully traverses and also respectfully disagrees with the characterization that the construction and structure of the circuitry disclosed in either reference and/or the functionality of the disclosed circuitry and the components thereof disclose the claimed invention as well as that *neither* reference provides any motivation, suggestion or teaching to modify the circuitry disclosed in Suzuki so as to yield the invention claimed by Applicant.

Applicant claims, claim 1, a signal production circuit for producing a plurality of kinds of pulse signals as well as claims, claim 9, a display device including such a signal production circuit, which signal production circuit includes, *inter alia*: (1) *storage means* for storing, as digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals

between the rise and fall timings; and (2) *serial-to-parallel converter means* for reading the signal of serial data from the storage means and producing, as parallel data, the plurality of kinds of pulse signals from the data representative of all the predetermined rise and fall timings of the plurality of kinds of pulse signals. It necessarily follows from the foregoing that the storage means is operably coupled to the serial-to-parallel converter means such that the signal of serial data stored in the storage means is passed to and received by the serial-to-parallel converter means such that the signal of serial data is converted within the converter so as to produce the plurality of parallel signals there from.

In accordance with the teachings and disclosures of the present invention, a single signal of serial data is produced by combining data representative of the rise and fall timings of each pulse signal and data representative of time intervals between all rise and fall timings and arranging same as a time series and this single signal of serial data is storage in the *storage means.* Thus, and as explained in the subject application, that part of the data that represents overlapping pulse signals as a time series can be omitted, and this consequently reduces the total quantity of data stored in the *storage means*, compared to the storing of all data as is required with conventional techniques, and the required data transfer rate. Further, only single signal of serial data is read from the *storage means*. Consequently, the number of terminals and data output lines of the *storage means,* for example, ROM, can be reduced to one.

The grounds for the rejection of the claims do not make clear whether it is the control circuit 103 or whether it is the latch circuit 105, as disclosed and taught in Suzuki, that corresponds to the storage means of the present invention. Thus, Applicant have included

comments as to why the control circuit 103 and the latch circuit 105 of Suzuki do ***not*** correspond to the storage means as set forth in claim 1 of the present invention as well as why the circuitry disclosed and taught in Suzuki cannot correspond to the circuitry as set forth in claim 1.

In contrast to the present invention, Suzuki discloses circuitry that includes a shift register 104 that is operably coupled to the latch circuit 105 and a control circuit 103 (see also Figure 14 thereof). In addition, the shift register 103 receives externally applied image data 5000. It also is described in Suzuki that the shift register *operates* based upon the control signal (shift clock) Tsft which enters from the control circuit. See Suzuki, col. 13, lines 52-62. Suzuki also discloses that the latch circuit 105 is a memory circuit that stores one line of imaged data for a requisite period of time in accordance with the control signal Tmry sent from the control circuit. The data thus stored is outputted to a voltage modulating circuit. See Suzuki, col. 13, lines 62-67.

As indicated above, in the presently claimed invention, the serial data that is to be converted is that contained in the signal that is stored in the storage means. There is no discussion anywhere in col. 13 of Suzuki that teaches or suggests that the control signal Tsft from the control circuit 103 comprises serial data that is to be converted in the shift register. To the contrary, it is clear from the discussion in Suzuki that the shift register 104 in Suzuki *operates* based upon this control signal.

It is clear from Suzuki and the foregoing discussion that the control circuit 103 in Suzuki, while it may output a control signal Tsft to the shift register 104, this control signal is NOT converted to a plurality of parallel signals in the shift register that are outputted from the shift register. Rather it is clear from this discussion in col. 13 of Suzuki that what is being converted is the image data being externally applied.

Moreover, it is clear from the foregoing discussion in Suzuki as well as that shown in Figure 14 thereof, that the control circuit 103 outputs four separate control signals therefrom respectively to shift register 104 (Tsft), to the latch circuit 105 (Tmry), to the voltage modulating circuit 106 (Tmod) and to the scanning circuit 102 (Tscan). As discussed in the subject application at pages 11-19 thereof a signal production circuit can be employed to produce a plurality of more control signals (pulse signals) to drive in a predetermined sequence a capacitive flat matrix display, for example. It is clear from the discussion in the subject application and the figures relating to this discussion, that the plurality or more control signals are produced from a stored signal of serial data instead of from a plurality of stored parallel and likely overlapping signals. It is thus clear that the control signal circuitry shown and described in Suzuki nowhere describes a process by which the four control signals are generated from a single serial data signal.

It also is clear from the discussion in Suzuki that the latch circuit 105 does not store data therein and supply such stored data *to* the shift register 104. Rather it is abundantly clear from Figure 14 of Suzuki, and the related discussion in col. 13 thereof, that the converted image data of one line of the image is *outputted to* the latch circuit 105. Thus, the latch circuit 105 cannot correspond to the storage means of the present invention as it is electrically impossible for data to flow from the latch circuit 105 to the shift register 104 in Suzuki. Moreover, such a re-arrangement of the circuitry disclosed in Suzuki would necessarily mean that the re-arranged circuitry would be unable to perform the intended function nor operate in the intended manner for the circuitry described in Suzuki.

Therefore, Suzuki nowhere discloses, teaches or suggests expressly or inherently the signal production circuit as set for in claim 1, nor the display device of claim 9. It is further submitted that Suzuki nowhere provides any suggestion, teaching or offer any motivation for modifying the signal circuitry disclosed therein so as to yield the signal production circuitry or display device of either of claims 1 or 9.

As to the secondary reference, Yamaguchi, this reference appears to be used for the limited person of teaching a specific shift register as shown in Figure 13 thereof. It is respectfully submitted that even if the shift register of Yamaguchi was combined with the other circuitry disclosed in Suziki, such a combination still would *not* yield the signal production circuitry claimed by Applicant. The as-revised circuitry resulting from the combination still would *not* yield the particular circuit arrangement or configuration of the storage means and the serial-to-parallel converter means as set forth in claim 1 of the present invention.

Applicant also would note that a notable feature of the present invention is the effective use of data by means of special serial-to-parallel conversion. Although a serial-to-parallel conversion circuit is disclosed in both Suzuki and Yamaguchi, the disclosed circuits are totally different from the conversion circuit of the present invention in conversion method.

The conversion method of the present invention is explained herein using Figs. 6(a), 6(b) of the present invention as an example (a copy of these figures is attached herewith for the Examiner's convenience). In the present invention, serial data (MDATA) is fed to each clock (CK) input of a shift register. The flip-flop outputs (data) are converted from 32-bit serial data to 4 parallel sets of

32-bit serial data (4x32=128 bits in total) by combinations of flip-flops and AND/OR logic circuits. The 4 sets of data are identified as SC, SU, SD, AL in the figures.

In contrast to the present invention, the serial-to-parallel conversion described by Suzuki and Yamaguchi is commonplace. Therein the serial data is supplied to the data (D) input of the first stage of a shift register, shifted according to a data transfer clock, and latched when transferred 32 clock times, for conversion to 32-bit parallel data (see also Figure A attached hereto).

In short, in the present invention: *32 serial bits→4 sets of 32 serial bits (= 128 bits)* whereas for Suzuki/Yamaguchi: *32 serial bits→32 parallel bits (= 32 bits)*. In addition, the present invention uses the original data 4 times more efficiently in the case of the example. The efficiency may be further raised in accordance with the number of generated signals. It is thus respectfully submitted that, the serial-to-parallel conversion circuit of the present invention completely differs from the conversion circuit of Suzuki and Yamaguchi.

In addition, and as can be seen from Figure 13 of Yamaguchi, the overall arrangement of the related functional elements of that circuitry disclosed in Yamaguchi is essentially the same as that disclosed and described in Figure 14 of Suzuki. As with Suzuki, in Yamaguchi the data being converted in the shift register 104 is the luminance signal component of the image as corrected by a gamma correction circuit 108. Consequently, Yamaguchi does not disclose, teach or suggest the signal production circuit as claimed by Applicant, as set forth in claim 1, nor the display device claimed by Applicant and as set forth in claim 9. Moreover, it is clear that Yamaguchi cannot teach, suggest or offer any motivation for modifying the circuitry disclosed in Suzuki so as to yield the signal production circuitry of claim 1 or the display device of claim 9.

Moreover, the above-referenced Office Action makes no reference in either of the two cited references why the suggested modification would be reasonably successful nor is any reference or assertion made in the Office Action that the suggested modification would not alter that intended function or operation of the circuitry and devices disclosed in Suzuki. In fact, and as indicated above the suggested modification to the circuitry as set forth in Fig. 14 of Suzuki would alter the intended function and operation of that circuitry and thus such a modification clearly is not allowable for purposes of forming a grounds for rejection.

The above-referenced Office Action also asserts that Yamaguchi teaches a memory incorporating waveform characteristics including a "rise time Tr" and a "fall time Tf". It is not clear from the content of the Action whether this means that the memory in Yamaguchi is being considered as equivalent to the storage means of the present invention. However, out of an abundance of caution, Applicant makes the following additional observations regarding Yamaguchi, which also shows that Yamaguchi does ***not*** disclose, teach or suggest an arrangement or feature that corresponds to the storage means of the present invention.

The above-referenced Office Action refers in particular to, col. 15, lines 47-67 of Yamaguchi. The memory discussed in this portion of Yamaguchi is not a memory as a storage device, but as a "memory function" for an electron-emitting device. Yamaguchi does not anywhere teach, describe nor suggest a member that is termed a "memory."

Notwithstanding this, and supposing for arguments sake that "memory" as the term is used in the Office Action meant "memory function" and that the Examiner regarded the electron-emitting device as corresponding to the storage means of the present invention, which is unlikely as

previously discussed, the electron-emitting device constitutes a part of a display panel and is not related at all to other circuit components such as the shift registers 104. Applicant thus respectfully submits, therefore, that the memory of Yamaguchi does ***not*** correspond to the storage means of the present invention.

As indicated herein, the Office Action also asserts that Yamaguich describes the "rise time Tr" and the "fall time Tf." These terms in Yamaguchi refer to the time required for a pulse to rise/fall, as depicted in Fig. 9B of Yamaguchi. Thus, these terms in Yamaguchi are completely different from the "rise and fall timings" of the present invention as set forth in the claims and as more particularly described in the subject application. Thus, and for the foregoing reasons, Applicant respectfully submits that Yamaguchi does not and cannot teach an arrangement corresponding to the storage means of the present invention.

As to claims 2-8 and 10-13, these claims are considered to be allowable at least because of their dependency from claim 1 or claim 9, which claims as indicated above are considered to be allowable. Also, and as to claims 2-6, Applicant would note that the above-referenced Office Action appears to assert a correspondence with the claimed invention essentially because the cited reference performs an allegedly similar function. It is respectfully noted, however, that nowhere does the Office Action refer to a discussion or figure in Suzuki that describes or illustrates the particular structure set forth in the claims.

As provided in MPEP 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the

knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F. 2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F. 2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). As provided above, the references cited, alone or in combination, include no such teaching, suggestion or motivation.

Furthermore, and as provided in MPEP 2143.02, a prior art reference can be combined or modified to reject claims as obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 19866). Additionally, it also has been held that if the proposed modification or combination would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. Further, and as provided in MPEP-2143, the teaching or suggestion to make the claimed combination and the reasonable suggestion of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As can be seen from the forgoing discussion regarding the disclosures of the cited references, there is no reasonable expectation of success provided in the references. Also, it is clear from the foregoing discussion that the modification suggested by the Examiner would change the principle of operation of the circuitry disclosed in Suzuki.

As the Federal circuit has stated, "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260,1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). Obviousness may not be established using hindsight or in view

of the teachings or suggestions of the inventor. *Para-Ordance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.2d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995).

The Federal Circuit also has indicated that a prior art reference that gives only general guidance and is not all that specific as to particular forms of a claimed invention and how to achieve it, may make a certain approach obvious to try, but does not make the invention obvious. *Ex Parte Obukowicz*, 27 USPQ2d 1063, citing *In re O'Farrell*, 853 F.2d 894, 7 USPQ2d 1673,1681 (Fed. Cir. 1988).

It is respectfully submitted that for the foregoing reasons, claims 1-13 are patentable over the cited reference(s) and, therefore, satisfy the requirements of 35 U.S.C. §103. As such, these claims are allowable.

CLAIMS 14-21

As indicated above, claims 14-19 were added to more distinctly claim embodiments of the present invention and claims 20-21 were added to more distinctly claim aspects/ embodiments of the present invention. These claims are clearly supported by the originally filed disclosure, including the originally filed claims. It also is respectfully submitted that these added claims are patentable over the cited prior art on which the above-described rejection(s) are based.

It is respectfully submitted that the subject application is in a condition for allowance. Early and favorable action is requested.

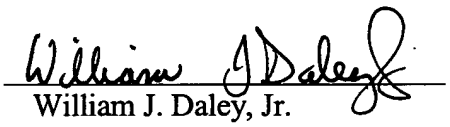
Although claims were added to the subject application, Applicant believes that additional fees are not required. However, if for any reason a fee is required, a fee paid is inadequate or credit

is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge

Deposit Account No. **04-1105**.

Respectfully submitted,
Edwards & Angell, LLP

Date: July 22, 2003

By: 

William J. Daley, Jr.
(Reg. No. 35,487)
P.O. Box 9169
Boston, MA 02209
(617) 439- 4444